U 4078 B

Tone ringer interface with dc-to-dc converter

Description

The tone ringer interface with dc/dc converter U 4078 B is an integrated circuit realized in bipolar technology, which allows high efficient power transfer. Galvanic separation takes place at Pin 5 either with inductive or opto–coupler mode.

Features

- Suitable for the specification: FTZ, 1TR2 and ETR2
- Rectifier bridge
- Z-diode
- Amplitude detection
- Detection of ringing signal i.e., sine-, triangle-, or rectangular (tone ringing) signal
- High-voltage bipolar technology
- Compact surface mount package (SO-8)

Benefits

- High efficient power transfer

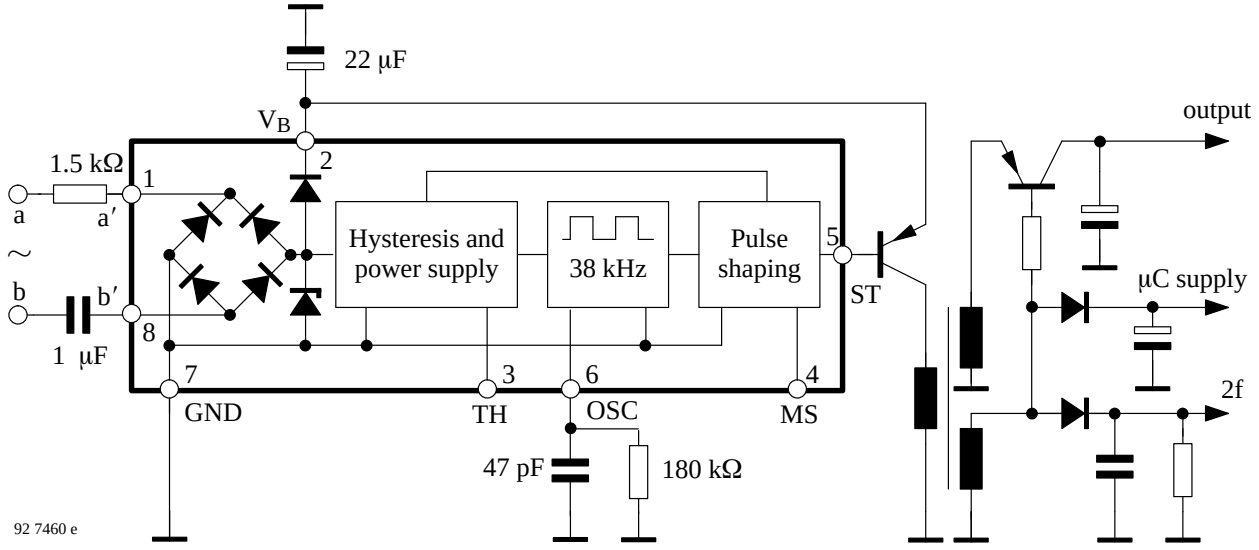

Figure 1. Block diagram with external circuit

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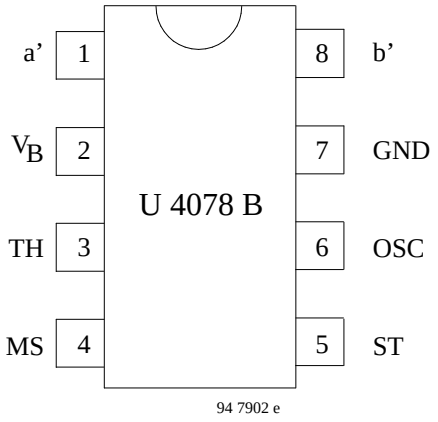
Pin Description

Pin	Symbol	Function
1, 8	a′, b′	AC ringing signal input
2	V_B	Output to charging capacitor (for supply)
3	TH	Comparator threshold adjustment input
4	MS	Mode selection: inductive or opto-coupler mode
5	ST	Switching transistor connection
6	OSC	RC circuit for internal oscillator input
7	GND	Ground



Functional description

The ringing ac signal, supplied by the exchange via lines a, b, is identified by a comparator circuit. An integrated oscillator, generates a 38 kHz clock signal, f_{clock}, via a coupled 2:1 divider. With the help of the external RC circuit, oscillation frequency is set at Pin 6. A PNP–transistor connected at Pin 5 enables the power transmission (transfer) in inductive or opto-coupler mode, which is selected at Pin 4. For inductive mode, Pin 4 is open, whereas for opto-coupler mode, Pin 4 is connected to GND (Pin 7).

Pin 1,8: Power Supply – a′, b′

Pins 1 and 8 connect the circuit with the ac ringing signal supplied by the exchange via lines a and b. A 1µF decoupling capacitor of 1 µF value together with a series resistance (1.5 kΩ) protect the circuit from overload across Pins 1 and 8. The circuit features the following overload protection across the a′, b′ terminals:

1) It can withstand a voltage of 110 V @ 50 Hz for maximum time of 15 seconds.

2) Testing of the circuit according to figure 2 does not destroy the circuit under following conditions:

Charging voltage of surge capacitance: V_{CS} = 2 kV
Pulse shape: 10/700 µs
Pulse sequence: 30 s
No. of surges: 10
Polarity change after 5 surges

Pin 2: Charging Capacitor (power supply filtering)

After the rectification of the ringing ac signal across the bridge circuit, the smoothing of the power supply is provided by the external capacitance at Pin 2 (22 nF).

Pin 3: Comparator Threshold − TH

Comparator threshold – as regards the ringing voltage – is set at ca. 12.5 V. Switching threshold can be increased or decreased by connecting a resistance at Pin 3 w.r.t. GND.

Pin 4: Mode Selection − MS

The ringing ac signal transfer (transmission) without potential loss occurs either via an inductive or opto-coupler mode. Pin 4 is set to a high state by an internal power source of 4 µA (approximately). This switches the output (Pin 5) to an operating state for the inductive mode. In case of opto-coupler mode, Pin 4 is connected to the ground (Pin 7).

Pin 5: Switching Transistor Connection

An external PNP transistor, whose emitter is at V_S (Pin 2) potential, serves to control the inductive or opto-coupler mode by connecting the base of the transistor with Pin 5.

In case of inductive mode, the signal, f_{clock} is interrupted for the duration of $t_{pulse} = 32/f_{clock}$, with every transition (rise or fall) of the ringing ac signal, f_{ring}. During the interruption, the setting at Pin 5 is such that the coil is critically damped (attenuated), whereas a current of 10 µA flows when the transistor at Pin 5 is switched on during the following t_{pulse} up to the next edge of the pulse.

In case of opto-coupler mode, the external transistor is switched on for a period of $t_{pulse} = 32/f_{clock}$ with every flank of the pulse of f_{ring}.

Pin 5 is at high resistance upto the next edge (flank) of the transition pulse of the ringing ac signal.

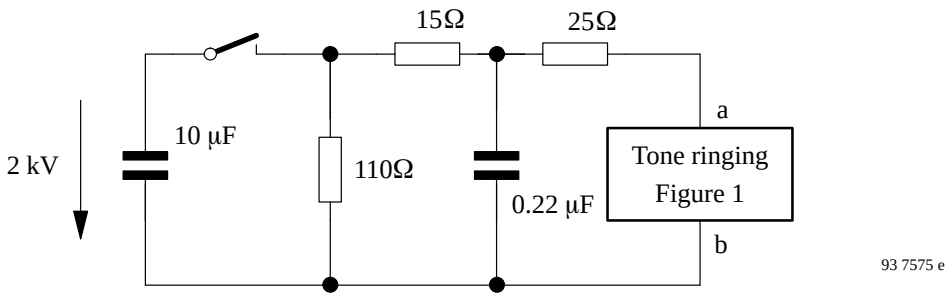


Figure 2

Absolute Maximum Ratings

Reference point Pin 7, unless otherwise specified

Parameters	Symbol	Value	Unit
Supply current Pin 1, 8	I_s	50	mA
Ambient temperature range	T_{amb}	–10 to + 60	°C
Storage temperature range	T_{stg}	–40 to + 125	°C
Power dissipation T_{amb} = 60 °C	P_{tot}	360	mW
Junction temperature	T_j	125	°C

Thermal resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	180	K/W

Electrical Characteristics

Reference point Pin 7, T_{amb} = –10 to + 60°C, V_B = 15 V, unless otherwise specified

Parameters	Test Conditions / Pin	Symbol	Min	Typ	Max	Unit
Supply current	f_{osc} = 65 to 87 kHz Pin 1, 8	I_s		420	500	µA
Threshold voltage for slope identification	Pin 3 open	V_{TH}	10	12.5	15	V
Audio impedance	f = 300 to 3400 Hz $V_{1,8} = 1 \cdot 5\ V_{rms}$	R	200			kΩ
Internal voltage limitation	I_z = 1 mA	V_z	26	30	32	V
Leakage current	1. phase Pin 5 2. phase	i_5 i_5	100 150			µA µA
Base current (PNP open)	Pin 5	$I_{B(5)}$	7	10	13	µA
Oscillator frequency range	Pin 6	f_{osc}	32.5	38	48.5	kHz
Duty-cycle	Pin 6		0.67	1		
Interrupted (pause) time of the output signal				$32/f_{clock}$		

Time sequence

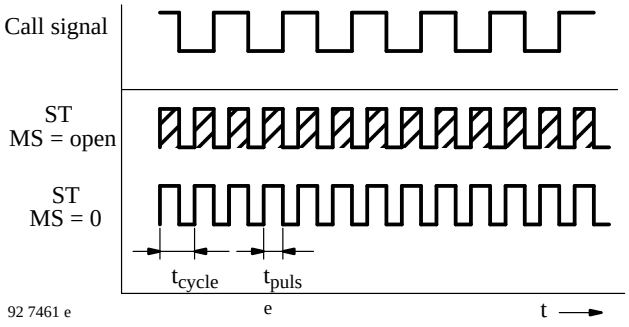
Internal clock frequency without RC tolerance

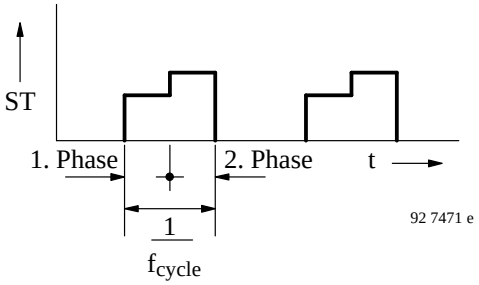
t_{clock} During this time, a clock signal is given at Pin 5 (ST).Pin 4 is open or ST is high ohmic. (MS=GND)

t_{pulse} By every polarity change of the call signal and MS open, the clock signal is interrupted for a time duration $t_{pulse} = 32/f_{clock}$. During interruption, the signal at ST (Pin5) is of such a value that the coil is critically attenuated (damped).

I_S (PNP) = $I_{ST} \approx 10\ \mu A$

A current of $I_{ST} \leqq 150\ \mu A$ is drawn from Pin 5 (ST) by every polarity change whereby MS is grounded.





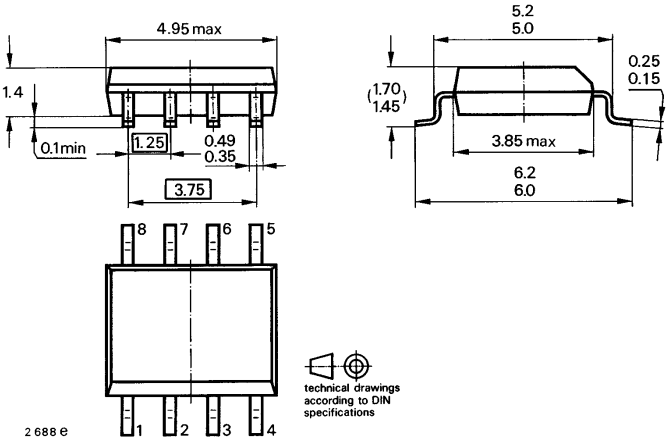
Current sequence at Pin 5 with an external PNP transistor connected as shown in figure 1. (f_{clock} = 38 kHz)

Order Information

Package	Type
SO 8	U 4078 B-FP

Dimensions in mm

Package: SO 8



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